User's Guide

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For Safety information, Warranties, and Regulatory information, see the pages behind Appendix A

Agilent Technologies E2487A Preprocessor Interface for Intel IA-32 Processors

The Agilent Technologies E2487A Preprocessor Interface — At a Glance

The Agilent Technologies E2487A Preprocessor Interface, when used together with the Agilent Technologies 16505A Prototype Analyzer, provides an interface for state analysis for various Intel IA-32 processors which use the Intel Pentium® Pro bus protocol, such as the Intel Pentium ® II processor. The E2487A requires a processor-specific probe adapter to connect to the supported processors.

The E2487A is supported by the Agilent Technologies logic analyzers listed below. The E2487A Preprocessor Interface requires that the logic analyzer module is in an Agilent Technologies 16500B/C mainframe; the 16505A Prototype Analyzer is also required.

> For instruction disassembly, Branch Trace Messages must be enabled and caches must be disabled. This requires a Pentium® II run-control tool (such as the Agilent Technologies E3493B) and a 30-pin debug port on the target system.

Logic Analyzer	**16500B Software Version**	**16500C Software Version**	**Channel Count**	**State Speed**	**Timing Speed**	**Memory Depth**
16550A (two card)	v3.09	v1.03	204	100 MHz	250 MHz	4 k states
16555A (three card)	v3.13	v1.03	204	110 MHz	250 MHz	1 M states
16555D (three card)	v3.13	v1.03	204	110 MHz	250 MHz	2 M states
16556A (three card)	v3.13	v1.03	204	100 MHz	200 MHz	1 M states
16556D (three card)	v3.13	v1.03	204	100 MHz	200 MHz	2 M states
16500B/C Mainframe	v3.13	v1.03				

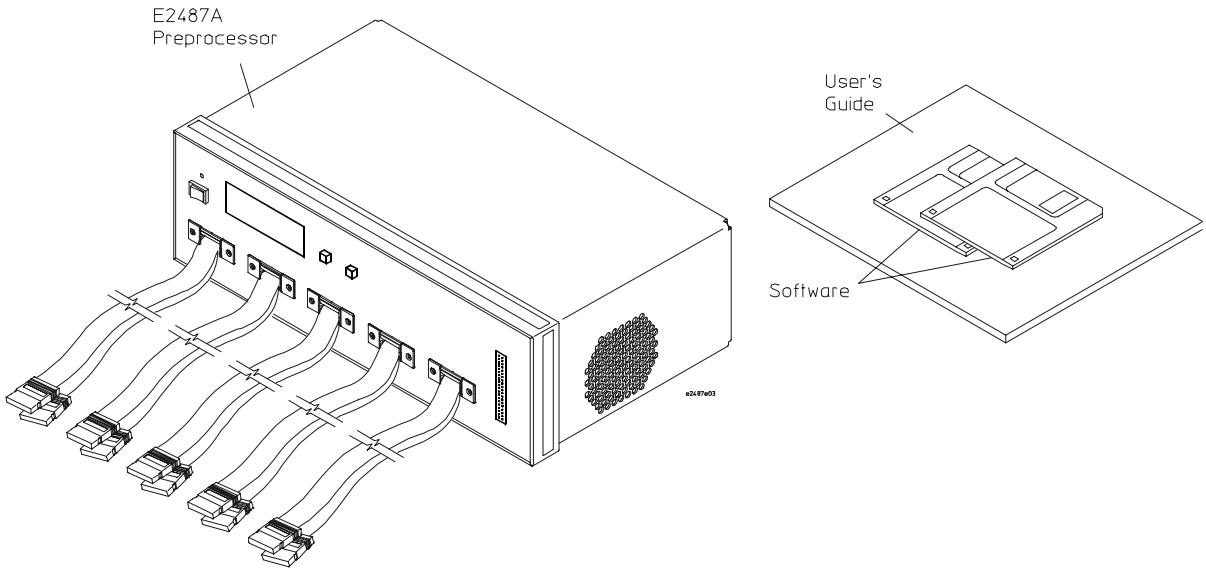
Additional Equipment	**Software Version**	
16505A Prototype Analyzer	A.01.30	
Agilent Technologies E3493B Processor Probe	v2.17	Provides Run Control connection to the target system. Refer to the *Agilent Technologies E3493B Processor Probe User's Guide* for operating instructions.

The E2487A Preprocessor Interface consists of the following:

- Configuration software, for configuring the logic analyzer and the 16505A Prototype Analyzer.
- The inverse assembler, which provides Intel IA-32 assembly language mnemonics for microprocessor activity. The inverse assembler also supports Intel's MMX™ Technology. A transaction tracker is also included.
- The preprocessor interface hardware, which processes the signals. The preprocessor interface hardware has front-panel cables for connecting the preprocessor interface to the probe adapter, and rear-panel connectors for the logic analyzer cables.

The preprocessor interface requires a probe adapter, which provides the physical connection to the target microprocessor. Contact your Agilent Technologies Sales Office for a list of supported processors and ordering information for the processor-specific probe adapters.

For more information on the supported logic analyzers, the 16505A, or the microprocessor, refer to the appropriate reference manuals for those products.



Agilent Technologies E2487A Preprocessor Interface

In This Book

This book is the user's guide for the Agilent Technologies E2487A Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters and one appendix:

Chapter 1 explains how to set up and configure the preprocessor interface and logic analyzer for state analysis.

Chapter 2 provides reference information on the logic analyzer format specification and symbols configured by the preprocessor interface software, and information about the inverse assembler.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

Contents

If You Have a Problem

1

Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the Agilent Technologies E2487A Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers. It also contains information on setting up the Agilent Technologies 16505A Prototype Analyzer for use with the IA-32 preprocessor interface.

Before You Begin

This section lists the logic analyzers supported by the Agilent Technologies E2487A, and provides other information about the analyzers and the preprocessor.

Equipment Supplied

- The preprocessor interface box.
- Configuration software for the Agilent Technologies 16500B/C Logic Analysis mainframe on a 3.5-inch disk.
- Transaction tracker and inverse assembly software for the Agilent Technologies 16505A Prototype Analyzer on a 3.5-inch disk.
- This User's Guide.

Minimum Equipment Required

- The Agilent Technologies E2487A IA-32 Preprocessor Interface, configuration files, and inverse assembly software.
- A processor-specific probe adapter.
- An Agilent Technologies 16505A Prototype Analyzer.
- One of the logic analyzers listed in the table on page ii, in an Agilent Technologies 16500B/C Logic Analysis Mainframe.

For instruction disassembly, Branch Trace Messages must be enabled and instruction caches must be disabled. This requires a run-control tool (such as the Agilent Technologies E3493B) and a 30-pin debug port on the target system. The Agilent Technologies E3493B run-control tool requires firmware version v2.17 or higher.

Setting Up the Preprocessor Interface Hardware

Setting up for the preprocessor interface hardware consists of the following major steps:

1. Turn off the power to the target system.

CAUTION

To protect your equipment, remove the power from the target system before you make or break connections. The preprocessor interface should always be powered up before the target system; when powering down, power down the target system first and then power down the preprocessor interface.

2. Install the probe adapter onto the target system microprocessor.

   Refer to the Installation Guide included with your probe adapter.

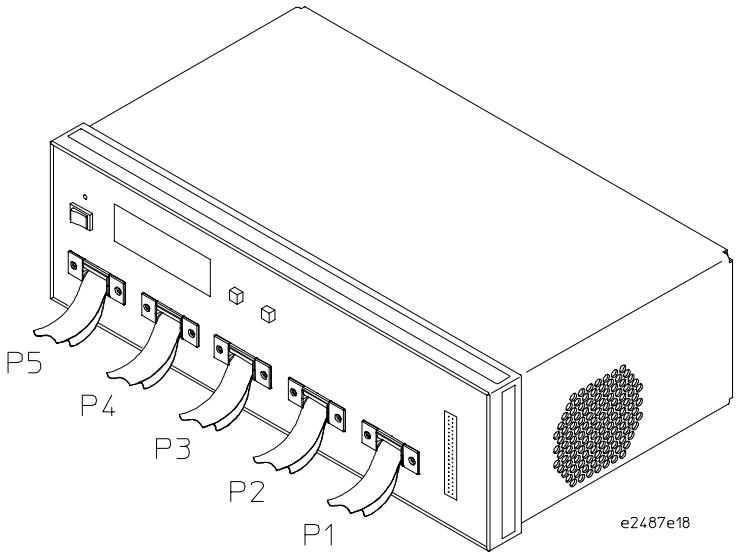
3. Connect the cables on the front of the preprocessor interface box to the connectors on the probe adapter.
4. Connect the logic analyzer cables to the connectors on the back of the preprocessor interface box.
5. Select the Operating Mode using the menu buttons on the front panel of the preprocessor interface box.

To install the probe adapter

The probe adapter comes with an Installation Guide. Refer to that manual for instructions for installing the probe adapter.

To connect the probe adapter to the interface box

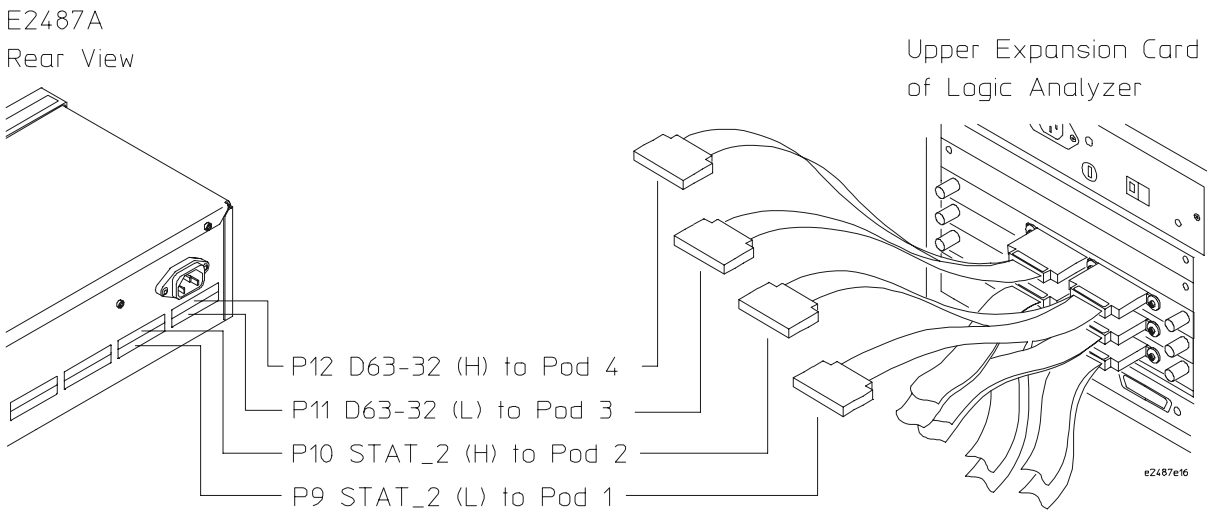
The preprocessor interface contains five connectors (ten pods) for connecting to the probe adapter. The illustration below shows the cables on the preprocessor interface hardware. Refer to the probe adapter Installation Guide for information on connecting the probe adapter to the interface box.



Probe Adapter Connectors on the Interface Box

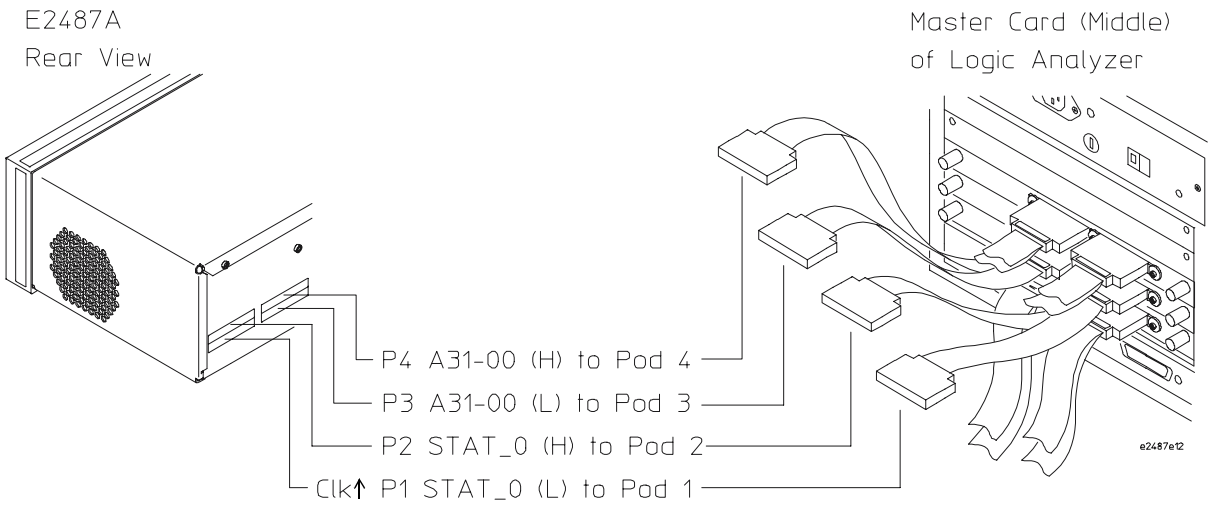
To connect to the 16555/56 analyzers

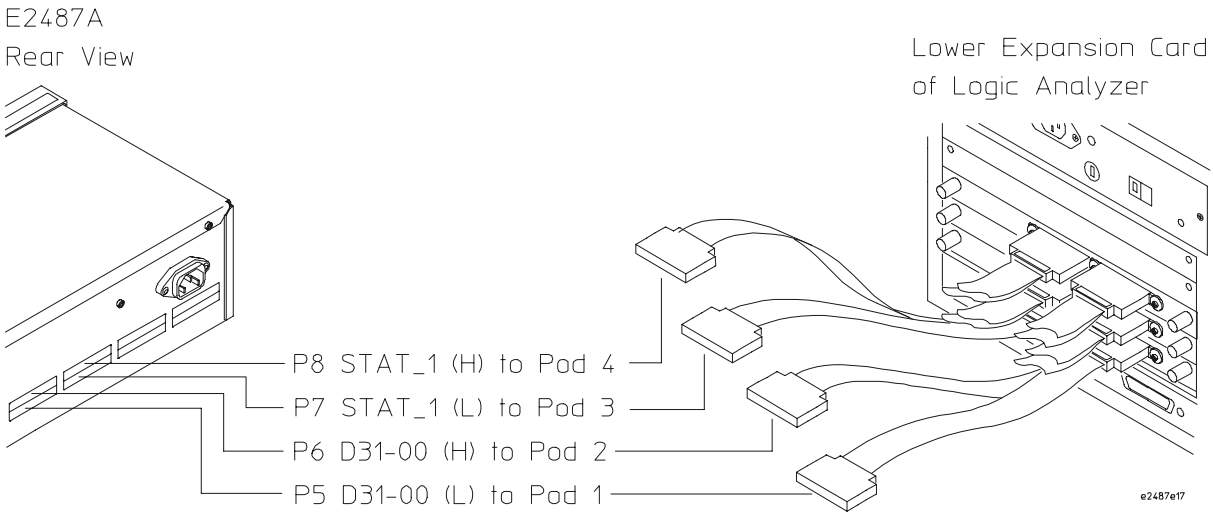
Use the following illustrations to connect to the Agilent Technologies 16555/56 logic analyzers.



Configuration file

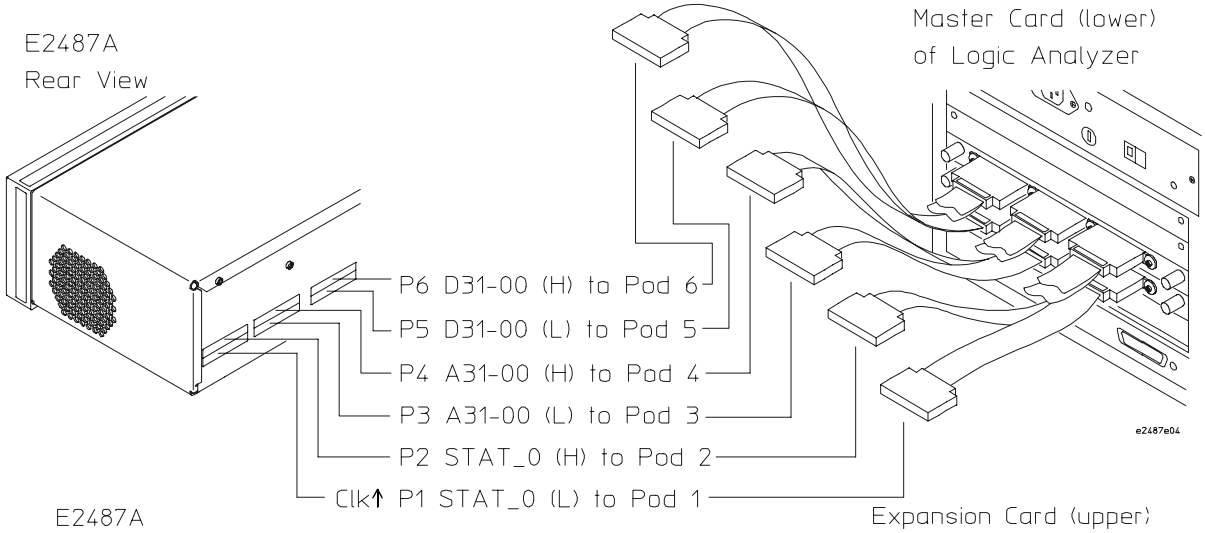
Use configuration file CP6D_1 for the Agilent Technologies 16555/56 Logic Analyzers.

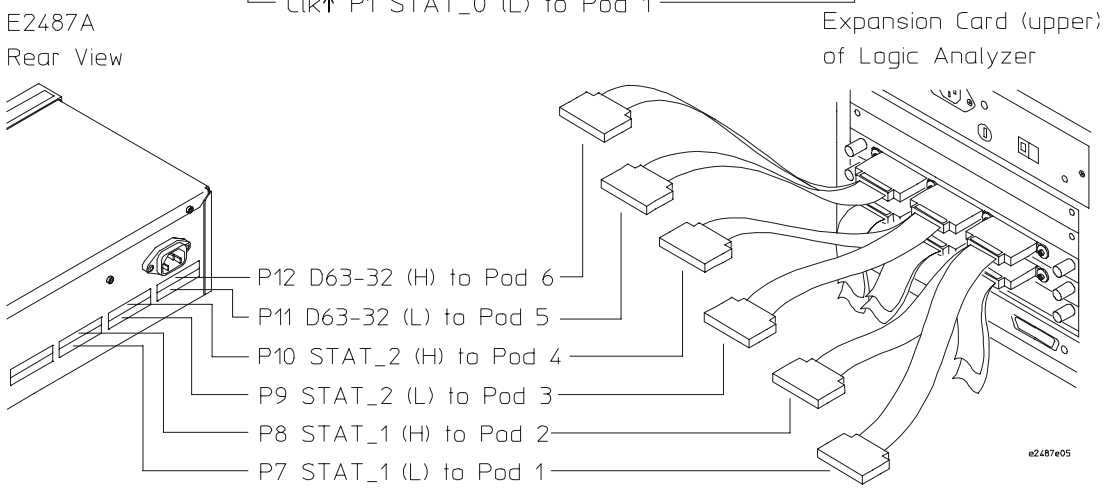

E2487A
Rear View
Master Card (Middle)
of Logic Analyzer
P4 A31-00 (H) to Pod 4
P3 A31-00 (L) to Pod 3
P2 STAT_0 (H) to Pod 2
Clk↑ P1 STAT_0 (L) to Pod 1
e2487e12


E2487A
Rear View
Lower Expansion Card
of Logic Analyzer
P8 STAT_1 (H) to Pod 4
P7 STAT_1 (L) to Pod 3
P6 D31-00 (H) to Pod 2
P5 D31-00 (L) to Pod 1
e2487e17

To connect to the 16550A analyzer

Use the following illustrations to connect to the Agilent Technologies 16550 logic analyzer.





Configuration file

Use configuration file CP6D_2 for the 16550A Logic Analyzers.

To power up or power down

When powering up, the logic analyzer, prototype analyzer, and preprocessor interface must be powered up first, and then the target system. Unpowered preprocessor interface circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer, prototype analyzer, and preprocessor interface.

To select the operating mode

The Agilent Technologies E2487A Preprocessor Interface provides two different modes of operation: State-per-clock with Expanded Clock Qualifier (STATE/CLK EXPANDED), and State-per-clock with Compacted Clock Qualifier (STATE/CLK COMPACTED). The mode of operation is displayed on an LCD display on the preprocessor interface box. A brief description of these modes is provided on the following page.

Two push-button switches on the front panel, "NEXT MODE" and "SELECT MODE", are used to change the operating mode. The NEXT MODE button is used to toggle between the available preprocessor modes. When the desired mode is displayed, press the SELECT MODE button. If the NEXT MODE or SELECT MODE button is not pushed within five seconds since the last time the NEXT MODE button was pushed, the preprocessor interface reverts to the last selected operating mode.

When the preprocessor is turned on, the current mode from previous use is displayed on the LCD display.

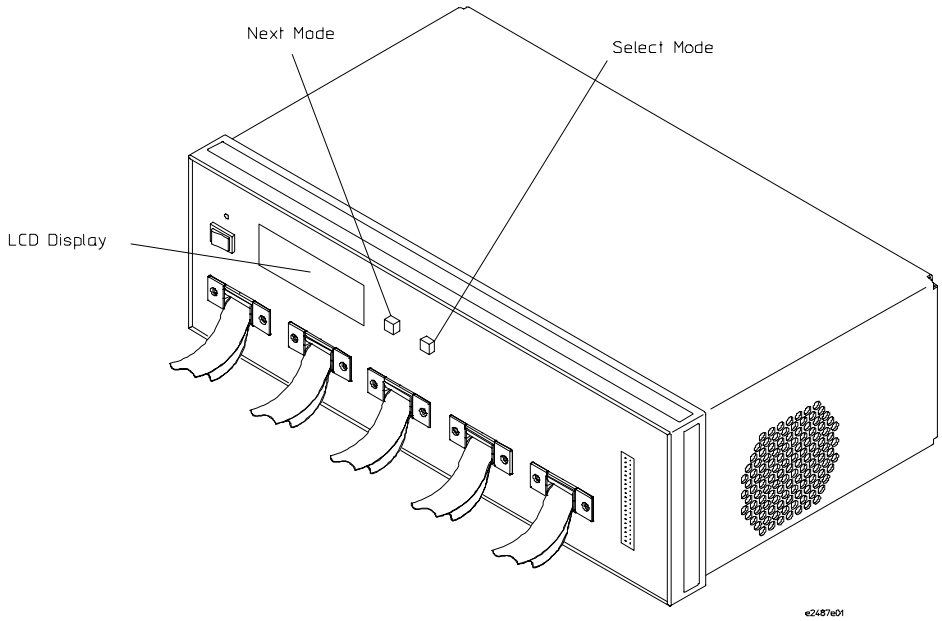
State-per-clock with Expanded Clock Qualifier

The Expanded clock qualifier acquires a state for every bus clock when there are transactions outstanding on the bus; no states are acquired when there are zero outstanding transactions.

State-per-clock with Compacted Clock Qualifier

The Compacted clock qualifier maximizes the number of transactions captured and is generally preferred.

Refer to Chapter 3, section "Modes of Operation", for more details on the preprocessor operating modes and clock qualifiers.



Preprocessor Interface Box with LCD Display and Mode Switches

Setting Up the Preprocessor Interface Software

The preprocessor interface software consists of one Agilent Technologies 16500B/C Logic Analysis System disk and one Agilent Technologies 16505A Prototype Analyzer disk. The 16500B/C disk contains logic analyzer configuration files; the 16505A disk contains the transaction tracker and the inverse assembler.

To copy the 16500B/C logic analyzer files

1. **The first time you set up the preprocessor interface, make a duplicate copy of the master disks.**

   For information on duplicating disks, refer to the reference manual for your logic analyzer.

2. **Ensure that the Agilent Technologies 16500B/C mainframe and the logic analyzer module have the required software version of the operating system.**

   The version requirements are listed on page ii.

3. **Insert the "Agilent Technologies 16500B/C Logic Analyzer Configs" flexible disk in the disk drive of the Agilent Technologies 16500B/C.**
4. **Select the "System, Hard Disk" menu using the front panel touch screen.**
5. **Create a directory on the logic analyzer using the command sequence "Make Directory, new directory name: <name>, Execute".**
6. **Select the "System, Flexible Disk" menu. Copy all files to the directory on the hard disk using the command sequence "Copy, file: *, to:\<name> on: Hard Disk, Execute".**

   The logic analyzer will later be configured through the Agilent Technologies 16505A, using the files you have just copied onto the logic analyzer hard drive.

To load the 16505A Prototype Analyzer files

The Agilent Technologies 16505A Prototype Analyzer is required for transaction tracking and inverse assembly. To set up the prototype analyzer:

1. If you have not already done so, copy the logic analyzer files as described in the previous section.

   The Agilent Technologies 16500B/C files must be copied to the logic analyzer hard drive first for the 16505A to access them.

2. Connect the 16505A to the 16500B/C. Power up the 16500B/C first, then power up the 16505A.

   For information on connecting the 16505A, refer to the *Agilent Technologies 16505A Installation Guide*.

3. Ensure that the 16505A has software version A.01.30 or greater.

   You may check the 16505A system version from a running session. In the Main window, click Help, then click "On Version...".

4. Install the 16505A software for the IA-32 processor.

   Place the "16505A Prototype Analyzer" flexible disk in the disk drive of the 16505A. In the Session Manager window, select the **`Update`** button. The window should display

   Filegroup: pp_p6d
   Version: A.01.30.

   Click on Update/Install and respond to the question by clicking on OK. Wait for the Information dialog to confirm a successful installation. Click on OK to acknowledge, and Close the Update/Install window.

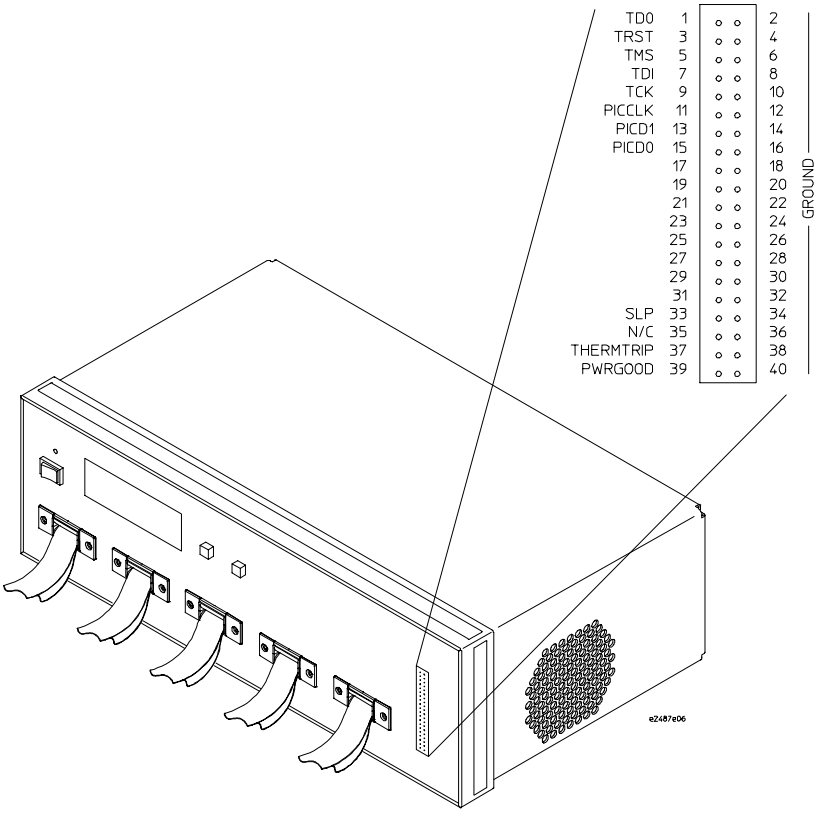
5. Load the logic analyzer configuration file.

   Start a session from the Session Manager window. When the main 16505A window opens, click on File in the top menu bar to get a pull-down menu, then click on "Load 16500 Files...". Change to the appropriate directory and load the appropriate file, either CP6D_1 or CP6D_2. Next, drag and drop the "IA-32" Instrument icon into the workspace area. Next, drag and drop a Listing Display on the "IA-32" Instrument icon in the workspace. Double click on the Listing icon to open the Listing window and verify that the label "IA-32 Inverse Assembly" appears.

To connect to the APIC and JTAG signals

The APIC and JTAG signals are routed to a 40-pin connector located on the front panel. These signals can be probed using the GP [General Purpose] probes that are shipped with your logic analyzer. The figure below shows the location of the connector and the signals on the connector. These signals are buffered versions of the system bus signals; they are not latched by the bus clock.

> Do not attempt to use the JTAG header as a run-control interface. This header is only capable of monitoring JTAG activity.



Analyzing the Intel IA-32 Processor

Analyzing the Intel IA-32 Processor

This chapter describes how to display configuration information and preprocessor interface data, gives label and symbol encodings for the status signal groups, and provides information about the transaction tracker and the inverse assembler, as displayed on the Agilent Technologies 16505A.

Displaying Information

This section describes how to display logic analyzer configuration information, state data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

To set up the 16505A workspace

To set up the Agilent Technologies 16505A workspace, drag and drop the "IA-32" Instrument icon into the workspace area. Next, drag and drop a Listing Display on the "IA-32" Instrument icon in the workspace. Double click on the Listing icon to open the Listing window and verify that the label "IA-32 Inverse Assembly" appears.

To display timing information

The Agilent Technologies E2487A does not support asynchronous timing analysis. However, you can view waveforms of timing relationships between signal transitions using the Waveform Display window. To capture these waveforms, set the operating mode to State-per-clock with Expanded Clock Qualifier, and turn off the clock qualifier using the Master Clock field in the Format menu.

To display the format specification

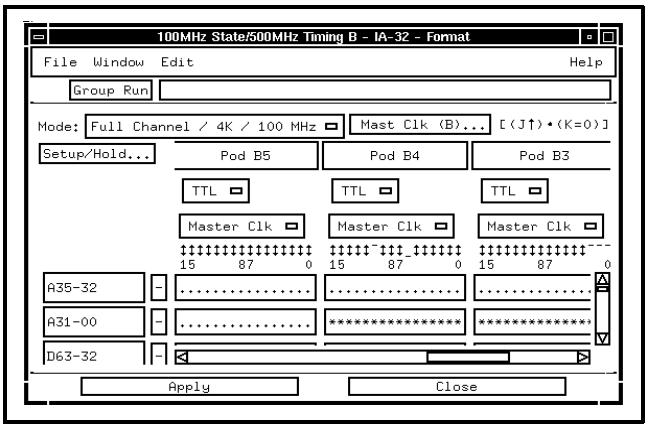
- **Using the mouse, right-click and hold on the instrument icon for the logic analyzer. In the pop-up menu, slide down to "Format..." then release the mouse button.**

  The Agilent Technologies E2487A configuration files contain predefined format specifications. These specifications include all labels for monitoring the microprocessor bus.

  Chapter 3 of this guide contains a table that lists the signals for the IA-32 processor and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection

information for your analyzer in chapter 1 to determine where the processor signals should be on the format specification screen.

The format specification display shown in the following figure is from the Agilent Technologies 16550A logic analyzer. Additional labels and pod assignments are listed off the screen. Scroll vertically to view additional signals. Scroll horizontally to view other pod-bit assignments. There may be some slight differences in the display for your particular analyzer.



Logic Analyzer Format Specification

To display the configuration symbols

- **Using the mouse, right-click and hold on the instrument icon for the logic analyzer. In the pop-up menu, slide down to "Symbol..." then release the mouse button. Choose a label name from the "Label" list, then select "User Defined Symbols...." The logic analyzer will display the symbols associated with the label.**

  The Agilent Technologies E2487A configuration software sets up symbol tables. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels simplify triggering on specific IA-32 processor cycles. The label base in the symbols menu is set to hexadecimal to conserve display space.

  All IA-32 system bus signals are routed to the logic analyzer probe headers or to extra headers. Labels that begin with a lower case letter are signals that are created by the preprocessor hardware; these signals are described more fully in chapter 3, "Modes of Operation". Labels that begin with an uppercase

letter and have lower case letters within them are signals that combine preprocessor generated signals and IA-32 processor signals.

The first of the following tables describes the IA-32 processor signals that are captured by the preprocessor. The second table lists the label and symbol encodings defined by the logic analyzer configuration software.

Note

Under the heading "Polarity", negative means that the logic analyzer inverts the signal. Positive means that the logic analyzer does not invert the signal.

Signal/Label List

Label Name	Polarity	Number of bits	Description
A20M#	positive	1	Address bit 20 Mask signal
A35-32	negative	4	Address bus bits 35:32
A31-00	negative	32	Address bus bits 31:00
ADS#	positive	1	Address Strobe
AERR#	positive	1	Address Parity Error signal
AP#	positive	2	Address Parity signals
BCLK	positive	1	Bus Clock signal
BERR#	positive	1	Bus Error signal
BINIT#	positive	1	Bus Initialization signal
BNR#	positive	1	Block Next Request signal
BP3#	positive	1	Breakpoint signal
BP2#	positive	1	Breakpoint signal
BPM1#	positive	1	Breakpoint and Performance Monitor signal
BPM0#	positive	1	Breakpoint and Performance Monitor signal
BPRI#	positive	1	Priority Agent Bus Request signal
BR#	positive	4	Symmetric Agent Bus request signals
D63-32	negative	32	Data bus bits 63:32
D31-00	negative	32	Data bus bits 31:00
DBSY#	positive	1	Data Bus Busy signal
DEFER#	positive	1	Defer signal
DEP#	positive	8	Data bus ECC/Parity signals
DRDY#	positive	1	Data Ready signal

FERR#	positive	1	Floating-point Error signal
FLUSH#	positive	1	Flush signal
Label Name	**Polarity**	**Number of bits**	**Description**
FRCERR	positive	1	Functional Redundancy Check Error signal
HIT#	positive	1	Snoop Hit signal
HITM#	positive	1	Snoop Hit Modified signal
IERR#	positive	1	Internal Error signal
IGNNE#	positive	1	Ignore Numeric Error signal
INIT#	positive	1	Initialization signal
INTR	positive	1	Interrupt Request signal
LINT	positive	2	Local Interrupt signals
LOCK#	positive	1	Bus Lock signal
NMI	positive	1	Non-maskable Interrupt signal
PRDY#	positive	1	Probe Ready signal
PREQ#	positive	1	Probe Request signal
RESET#	positive	1	Reset signal
RP#	positive	1	Request Parity signal
RS#	positive	3	Response Status
RSP#	positive	1	Response Parity signal
SMI#	positive	1	System Management Interrupt signal
STPCK#	positive	1	Stop Clock signal
TRDY#	positive	1	Target Ready signal

The following table lists the transaction type symbol encodings defined by the logic analyzer configuration software for the TranTy label.

IA-32 Processor Transaction Type Symbols

Signal	Symbol
TranTy	"Branch Trace" "Code Read " "Data Read " "Defer Reply " "Int Ack/Spcl" "Invalidate " "I/O Read " "I/O Write " "Mem Write " "RSVD_1 " "RSVD_2 " "RSVD_3 " "RSVD_4 " "Writeback " "--- "

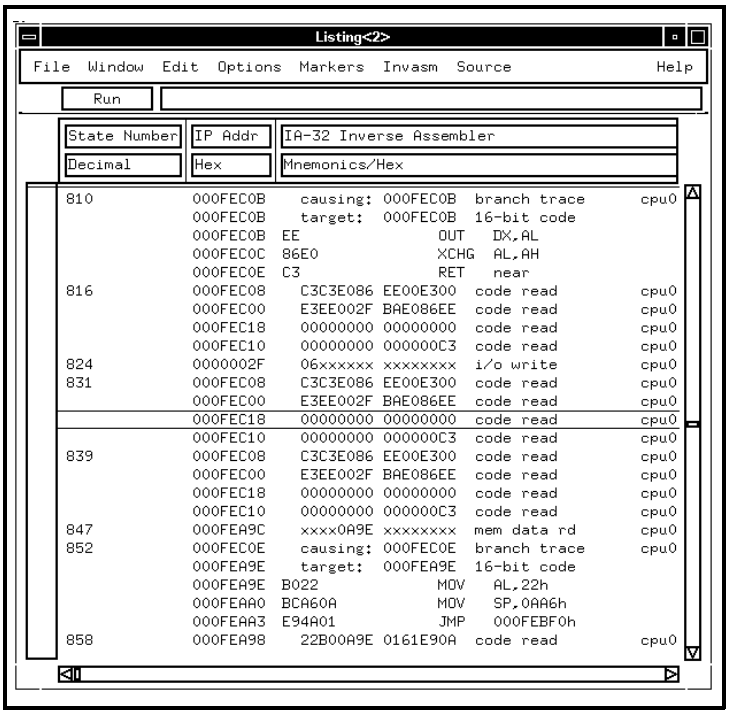
To display captured state information

The captured information is displayed in the Listing display.

- **Open the Listing display for your logic analyzer.**

  If your trace listing doesn't otherwise appear to be correct, make sure the logic analyzer is configured for state analysis and correctly connected. See Chapter 1 to review the logic analyzer connections, correct it if needed, and then run the trace again.

  The figure below shows the Listing display for the Agilent Technologies 16550A logic analyzer.



Logic Analyzer Listing Display

Using the Transaction Tracker

This section discusses the general output format of the transaction tracker, and any processor-specific information you will need.

The transaction tracker supports many filter options based on type of states (start of a transaction, all of a transaction), transaction types, and transaction-agent ownership. The next few paragraphs describe the general output format of the transaction tracker.

Data Format

The transaction tracker processes the captured data in a transaction-based format.

Numeric Format

For the data bus values, the numeric output from the transaction tracker is in hexadecimal format. All other numbers are in decimal format.

Filter options

The transaction tracker supports many filter options based on phases (start of a transaction, all of a transaction), transaction types, and transaction ownership. The following is a list of the filter options available.

Filterable State	**Options**
Show Phases	
Request Phase A:	Show/Suppress
All Phases:	Show/Suppress
Agents	
CPU 0:	Show/Suppress
CPU 1:	Show/Suppress
CPU 2:	Show/Suppress
CPU 3:	Show/Suppress
Priority:	Show/Suppress

Filterable State	Options
Show Transactions:	
Code Reads:	Show/Suppress
Memory Data Reads:	Show/Suppress
Mem Read & Invalidate:	Show/Suppress
Memory Writes:	Show/Suppress
Memory Writebacks:	Show/Suppress
I/O Reads:	Show/Suppress
I/O Writes:	Show/Suppress
Deferred Replies:	Show/Suppress
Interrupt Acknowledges:	Show/Suppress
Special Transactions:	Show/Suppress
Branch Trace Messages:	Show/Suppress

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The preceding section shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function gives you a better analysis display in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

Transaction tracker messages

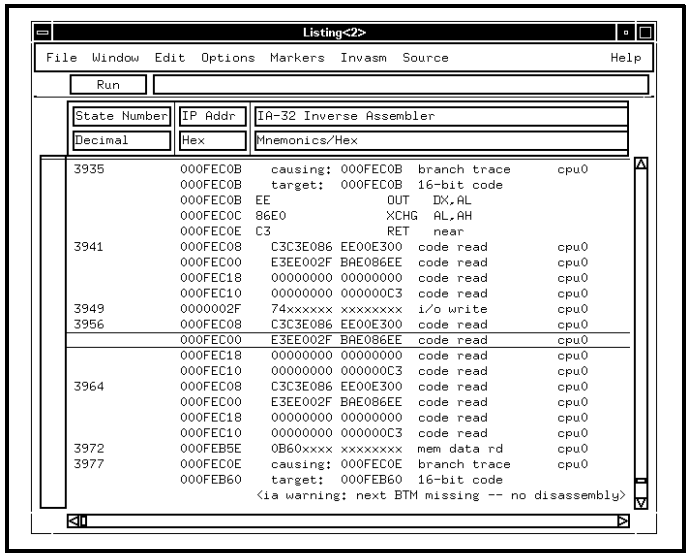
Any of the following messages may appear during analysis of your target software. Included with each message is a brief explanation.

Errors and warnings

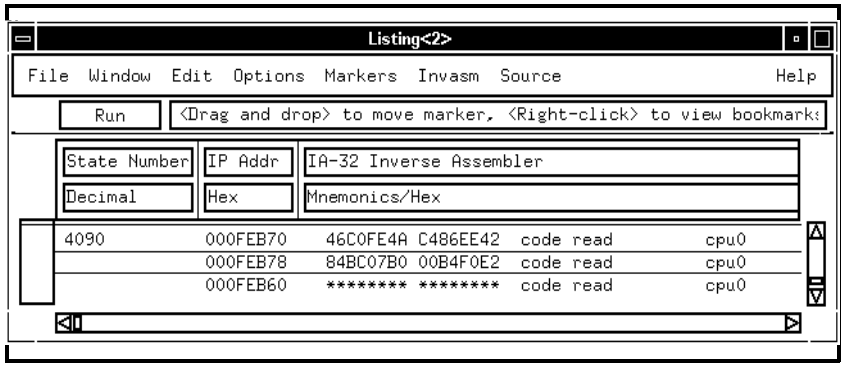
The Agilent Technologies E2487A software contains error messages and warnings for both the transaction tracker and the inverse assembler. For a list and description of the messages, refer to Appendix A.

Reaching boundaries

If the transaction tracker internal search limit (8192 states per transaction) is exceeded, or if part of a transaction is not acquired at the end of the analyzer acquisition memory, error messages may be displayed. The figure below shows a warning message. On the next page, the figure shows the end of a boundary.



Listing Display with Boundary Error Message



Listing Menu Showing End of Boundary

Protocol Violations

The transaction tracker displays a bus protocol violation when the maximum allowable outstanding transactions have been exceeded.

Protocol violations are followed with line:

"*** protocol violation detected ***"

The transaction tracker does not attempt to do a complete job of detecting protocol violations. Undetected protocol violations may cause the transaction tracker to display incorrect results.

Using the Inverse Assembler

In addition to basic transaction tracking, the Agilent Technologies 16505A can display an accurate instruction execution trace of IA-32 processor target systems containing up to four processors. Instruction disassembly supports Intel's MMX technology. Disassembly requires the use of a separate run-control tool such as the Agilent Technologies E3493A to disable all CPU caches and enable Branch Trace Message transactions.

Analysis features are determined by a combination of preprocessor interface operating mode settings and options selected in the 16505A Listing window under the "Invasm - Filter..." and "Invasm - Preferences..." menu pull-downs. The Filter dialog allows the user to show, suppress, or change the color of an entire acquisition state, whereas the Preferences dialog controls the display format for a state which is shown.

Disassembly is only possible when "Display Disassembly" is selected in the Preferences dialog and "Branch Trace Messages" are selected in the Filter dialog. Additionally, a run-control tool should be used to enable Branch Trace Messages and disable the instruction caches for all processors.

Operating mode

The inverse assembler software requires that the operating mode on the preprocessor interface hardware is set to one of the modes listed below.

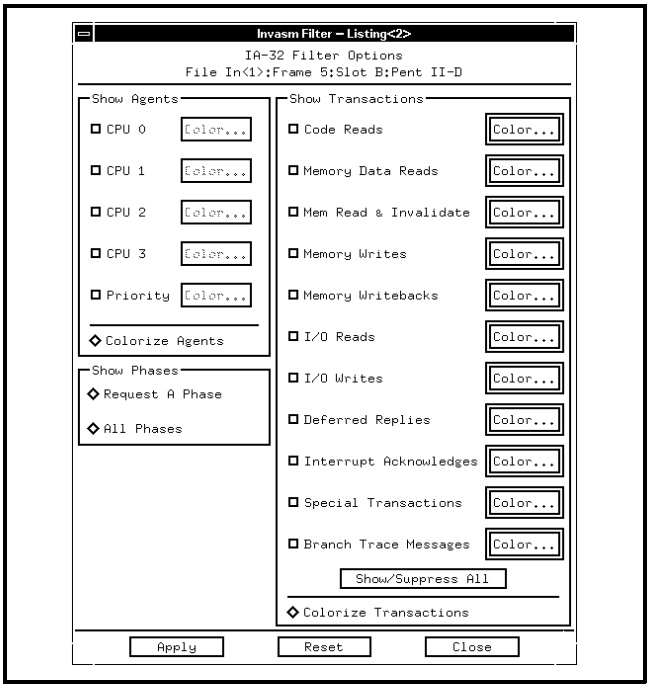
- State-per-clock Mode with Expanded Clock Qualifier
- State-per-clock Mode with Compacted Clock Qualifier

Refer to Chapter 1 for the mode selection procedure.

See Appendix A for a complete list of error messages.

IA-32 filter dialog

Filter options are accessed from the Listing menu bar by clicking on Invasm and selecting Filter. The Filter dialog provides the ability to display only information for particular bus agents and/or transaction types. Colorization can be used to identify either transactions or processors. Show Phases allows you to show only the Request A Phase, which contains a summary of the entire transaction, or All Phases, which includes all captured states pertaining to each transaction. The figure below shows a sample Filter dialog.



Agilent Technologies 16505A IA-32 Filter Dialog

IA-32 preferences dialog

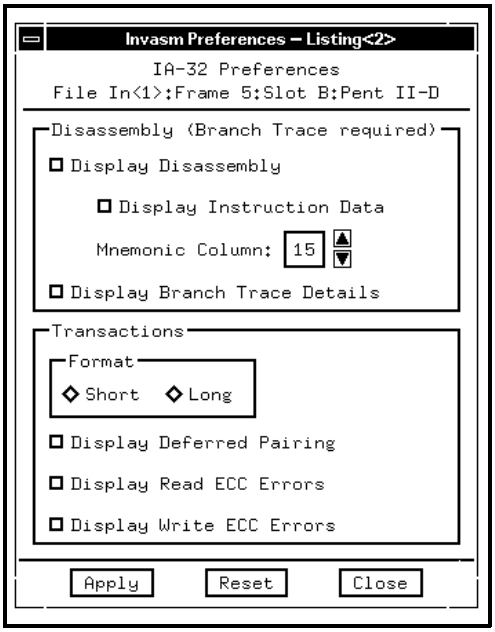
Preferences options are accessed from the Listing menu bar by clicking on Invasm and selecting Preferences. The Preferences dialog controls the level of detail for states shown. The figure on the following page shows the Preferences dialog.

Disassembly

When "Display Disassembly" is selected, a block of instructions appears in the Listing window under each Branch Trace Message transaction or Memory Code Read from the reset vector (the instruction cache(s) must be disabled). "Display Instruction Data" turns on/off the display of data bytes corresponding to each instruction. "Display Branch Trace Details" shows the causing and target linear addresses contained in each Branch Trace Message transaction, along with the default address/operand size.

Transactions

The transaction Format can be set to "Short" to display one line per transaction data chunk (DRDY# asserted state), or "Long" for more extensive information about the phases. "Display Deferred Pairing" consolidates the deferred reply transaction information directly beneath the original deferred transaction. "Display Read/Write ECC Errors" examines the D[63:00]# and DEP[7:0]# signals during DRDY# asserted states and displays detected errors not on the data phase, but on the Request phase which started the transaction. Bad bits are identified for single-bit correctable errors. These ECC options should only be selected when data bus error-checking is enabled on the target system. While CPU agents usually drive DEP[7:0]#, non-CPU agents may or may not, so exercise judgment when turning on "Display Read ECC Errors".



Agilent Technologies 16505A IA-32 Preferences Dialog

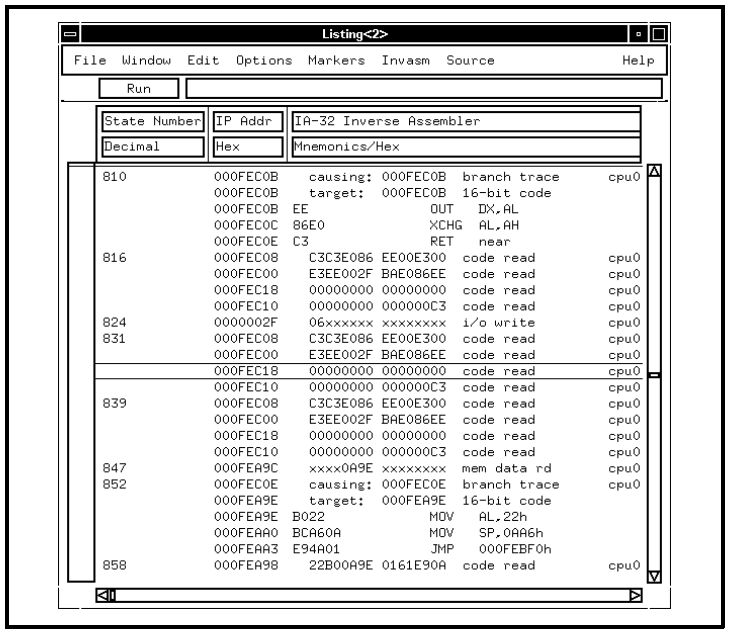
Analysis techniques

Suggested Settings

For software analysis, the settings below give a high-level view of the captured data. Remember to disable the processor instruction caches and enable Branch Trace Messages in order to get disassembly.

Operating Mode: State/Clock with Compacted Clock Qualifier.

Filter:	Show Agents	-- Show All
	Show Transactions	-- Show All except Code Reads
	Show Phases	-- Request A Phase
Preferences:	Display Disassembly	-- ON
	Display Branch Trace Details	-- ON
	Transaction Format	-- SHORT
	Display Deferred Pairing	-- ON
	Display Read ECC Errors	-- OFF
	Display Write ECC Errors	-- ON



Agilent Technologies 16505A Listing Window for Software Analysis

For hardware analysis, the State Waveform display provides the most relevant details. If this display does not provide the level of detail required for your analysis needs, you might need the restricted version of the Agilent Technologies E2487A. Contact your Agilent Technologies Sales Office for information on obtaining the appropriate Intel non-disclosure forms for the restricted version.

Disassembler Behavior

To display instruction disassembly, use an IA-32 processor run-control tool such as the Agilent Technologies E3493A to enable Branch Trace Messages and disable the processor instruction caches. Show "Branch Trace Messages" in the Filter dialog, and select "Display Disassembly" in the Preferences dialog.

When a processor executes a branching instruction, the prefetch queues are flushed, a Branch Trace Message (BTM) appears on the bus, and the processor begins fetching code at the branch target address. The disassembly software finds matching code reads between the current BTM and the next matching BTM, reorders any out-of-order bursts, then disassembles the code read data. In searching for code reads, any fetches which are deferred are automatically paired with their corresponding deferred replies to ensure that all code read data is found. This pairing is not affected by the "Display Deferred Pairing" setting in the Preferences dialog.

Physical vs. Linear Addresses

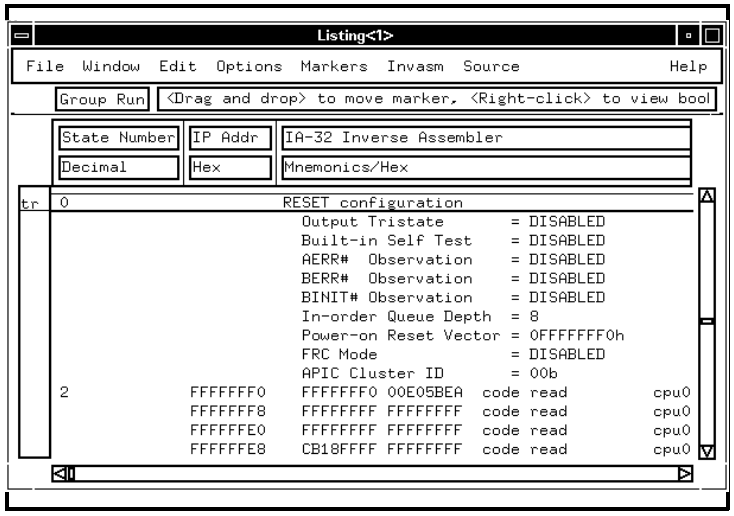
Branch Trace Messages give linear causing and target addresses. The addresses displayed for Memory Code Read transactions in the "IP Addr" column are physical. For real-mode programs, these linear and physical addresses are equivalent. For protected-mode programs with paging enabled, the address bits higher than A[11] will usually be different.

For disassembled instructions, linear addresses are shown in the "IP Addr" column of the Listing window.

The following table describes the reset configuration information that is displayed at reset.

Reset Configuration

Signal at Reset	Configuration (asserted/deasserted)
FLUSH#	Output Tristate Enabled/Disabled
INIT#	Built-in Self Test Enabled/Disabled
A8#	AERR# Observation Policy Enabled/Disabled
A9#	BERR# Observation Policy Enabled/Disabled
A10#	BINIT# Observation Policy Enabled/Disabled
A7#	In-order Queue depth = 1/8
A6#	Power-on Reset Vector = 000FFFF0 or FFFFFFF0 hex
A5#	FRC Mode Enabled/Disabled
A[12:11]#	APIC Cluster ID (00, 01, 10, 11)



Reset Configuration

Triggering Hints

Storage qualification

Clock qualification is a form of storage qualification. You can turn the clock qualifier off and capture all bus clocks; however, you should not attempt any other storage qualification using the trigger sequence, as that might result in error messages in the inverse assembly column in the Listing.

Triggering on address and transaction type

To trigger on a specific address and transaction type, use the A35-32, A31-00, and TranTy labels, together with the TranTy label symbols. The symbols identify each transaction type uniquely, except for Interrupt Acknowledge and Special Transactions, which are combined into one symbol.

Triggering on data and transaction type

There is no guaranteed method of triggering on a particular transaction type or address ANDed with a particular data value in a target system with overlapping transactions. Although the Listing displays a transaction type and 8-byte data value on the same line when Transaction Display Mode is set to Short, this alignment is the result of post-processing and cannot be used for triggering. The preprocessor interface hardware captures this information on different states. A trigger specification could be defined to find a certain transaction type in the Request A phase, then trigger on a data value qualified by DRDY# asserted; however, by the time the data pattern is found, it could belong to a different transaction.

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the Agilent Technologies E2487A hardware including the characteristics and signal mapping for the preprocessor interface. This chapter also includes a brief theory of operation, and information on servicing the preprocessor interface.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Operating Characteristics

Microprocessor Compatibility	Intel IA-32 microprocessors which use the Pentium Pro bus protocol, such as the Pentium II	
Microprocessor Package	Call Agilent Technologies for processors/packages supported	
Clock Frequency	100 MHz maximum for external BCLK	
Clock Duty Cycle	BCLK high time is 3.1 ns minimum at >1.7V. BCLK low time is 3.4 ns minimum at <0.7V.	
Target Signal Amplitude	800 mV p-p minimum for all GTL+ signals	
Logic Analyzers Supported	16550A (two card) 16555A/D (three card) 16556A/D (three card)	
Accessories Required	Probe adapter. Call Agilent Technologies for ordering information.	
Power Requirements	115/230 Vac, 160W Power supply is built into the preprocessor interface. CAT II, Pollution degree 2.	
Pods Required	Twelve logic analyzer pods are required.	
Signal Line Loading	Varies depending on probe adapter.	
Environmental Temperature	Operating Nonoperating	20 to 30 degrees C -40 to +70 degrees C
Altitude	Operating Nonoperating	4,600 m (15,000 ft) 15,300 m (50,000 ft)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Modes of operation

The preprocessor interface operates only in State-per-clock mode. The logic analyzer master clock is normally qualified with the "cqual#" signal from the preprocessor. This clock qualifier is set to either Compacted or Expanded. By eliminating idle clocks, the Compacted qualifier can potentially capture many more transactions than the Expanded qualifier. Refer to chapter 1 for information on configuring the preprocessor interface and logic analyzer for the desired mode of operation.

The preprocessor interface uses the BCLK rising edge to capture the signals from the IA-32 processor bus and to clock the logic analyzer. The PLDs in the preprocessor generate additional information about each clock. The PLD information along with the bus signals are sent to the logic analyzer and used by the transaction tracker and inverse assembler to produce the transaction display (see Block Diagram).

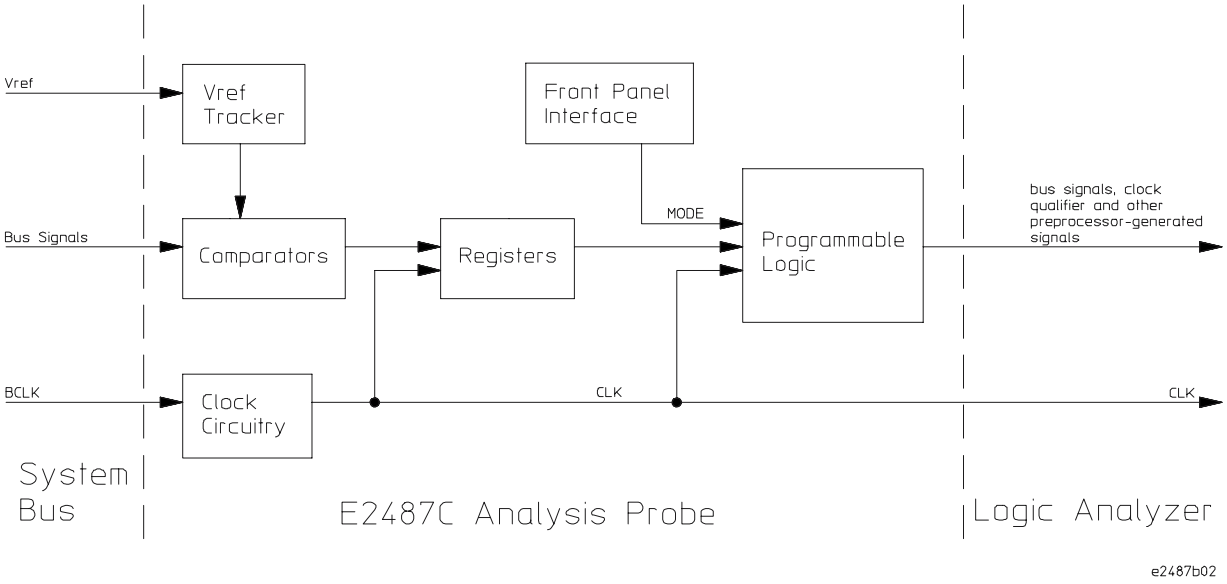
IA-32 processor signals require a multi-clock latency to move the information from the processor pins to the logic analyzer memory. The first clock is used to capture all of the bus signals in latches on the preprocessor. Subsequent clocks move the bus signals through the PLDs and into the logic analyzer.

The preprocessor interface captures but does not display the REQ[4:0]# bus signal group.

Clocking

The logic analyzer uses the master clock specification [(J↑) • (K = 0)] to capture all pod data. Connector P1 carries BCLK (J ↑), which clocks the logic analyzer. Connector P2 carries the "cqual#" (K = 0) signal from the PLD, which is used to qualify the master clock to eliminate the acquisition of unnecessary data. The qualifier is highly recommended, but not required.

Agilent Technologies E2487A Block Diagram



Agilent Technologies E2487A Block Diagram

Signal-to-Connector Mapping

The following table describes the electrical interconnections implemented with the Agilent Technologies E2487A Preprocessor Interface. Since the pods on the
logic analyzers are numbered differently than the preprocessor connectors, refer to the connection table in chapter 1 to correlate the pod numbers.

The signal list table column descriptions are as follows:

PREPROCESSOR CONNECTOR	NAME	The preprocessor connector that carries the signal.
	PIN	The pin within the preprocessor connector that carries the signal.
	BIT	The bit position of the signal within the preprocessor connector.
CPU	SIGNAL	The microprocessor signal name.
ANALYZER	LABEL(S)	The analyzer label assigned to the signal. Lower case letters indicate a preprocessor-generated signal.

IA-32 Signal List

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P1	3	CLK1	BCLK	BCLK
P1	7	D15	*	
P1	9	D14	*	
P1	11	D13	*	
P1	13	D12	*	
P1	15	D11	*	
P1	17	D10	*	
P1	19	D9	*	
P1	21	D8	*	
P1	23	D7	*	
P1	25	D6	*	
P1	27	D5	RS2#	RS#
P1	29	D4	RS1#	RS#
P1	31	D3	RS0#	RS#
P1	33	D2	DEFER#	DEFER#
P1	35	D1	HIT#	HIT#
P1	37	D0	HITM#	HITM#

* These signals are generated by the preprocessor interface.

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P2	3	CLK1	cQual#	cQual#
P2	7	D15	RESET#	RESET#
P2	9	D14	STPCLK#	STPCK#
P2	11	D13	BINIT#	BINIT#
P2	13	D12	INIT#	INIT#
P2	15	D11	BERR#	BERR#
P2	17	D10	TRDY#	TRDY#
P2	19	D9	DRDY#	DRDY#
P2	21	D8	DBSY#	DBSY#
P2	23	D7	ADS#	ADS#
P2	25	D6	*	
P2	27	D5	*	
P2	29	D4	*	
P2	31	D3	*	
P2	33	D2	*	
P2	35	D1	*	
P2	37	D0	*	

* These signals are generated by the preprocessor interface.

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P3	3	CLK1	FLUSH#	FLUSH#
P3	7	D15	A15#	A31-00
P3	9	D14	A14#	A31-00
P3	11	D13	A13#	A31-00
P3	13	D12	A12#	A31-00
P3	15	D11	A11#	A31-00
P3	17	D10	A10#	A31-00
P3	19	D9	A9#	A31-00
P3	21	D8	A8#	A31-00
P3	23	D7	A7#	A31-00
P3	25	D6	A6#	A31-00
P3	27	D5	A5#	A31-00
P3	29	D4	A4#	A31-00
P3	31	D3	A3#	A31-00
P3	33	D2	A2#*	A31-00
P3	35	D1	A1#*	A31-00
P3	37	D0	A0#*	A31-00

*These signals are tied high

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P4	3	CLK1	mQual *	mQual
P4	7	D15	A31#	A31-00
P4	9	D14	A30#	A31-00
P4	11	D13	A29#	A31-00
P4	13	D12	A28#	A31-00
P4	15	D11	A27#	A31-00
P4	17	D10	A26#	A31-00
P4	19	D9	A25#	A31-00
P4	21	D8	A24#	A31-00
P4	23	D7	A23#	A31-00
P4	25	D6	A22#	A31-00
P4	27	D5	A21#	A31-00
P4	29	D4	A20#	A31-00
P4	31	D3	A19#	A31-00
P4	33	D2	A18#	A31-00
P4	35	D1	A17#	A31-00
P4	37	D0	A16#	A31-00

* These signals are generated by the preprocessor interface.

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P5	3	CLK1	FRCERR#	FRCERR#
P5	7	D15	D15#	D31-00
P5	9	D14	D14#	D31-00
P5	11	D13	D13#	D31-00
P5	13	D12	D12#	D31-00
P5	15	D11	D11#	D31-00
P5	17	D10	D10#	D31-00
P5	19	D9	D9#	D31-00
P5	21	D8	D8#	D31-00
P5	23	D7	D7#	D31-00
P5	25	D6	D6#	D31-00
P5	27	D5	D5#	D31-00
P5	29	D4	D4#	D31-00
P5	31	D3	D3#	D31-00
P5	33	D2	D2#	D31-00
P5	35	D1	D1#	D31-00
P5	37	D0	D0#	D31-00

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P6	3	CLK1	FERR#	FERR#
P6	7	D15	D31#	D31-00
P6	9	D14	D30#	D31-00
P6	11	D13	D29#	D31-00
P6	13	D12	D28#	D31-00
P6	15	D11	D27#	D31-00
P6	17	D10	D26#	D31-00
P6	19	D9	D25#	D31-00
P6	21	D8	D24#	D31-00
P6	23	D7	D23#	D31-00
P6	25	D6	D22#	D31-00
P6	27	D5	D21#	D31-00
P6	29	D4	D20#	D31-00
P6	31	D3	D19#	D31-00
P6	33	D2	D18#	D31-00
P6	35	D1	D17#	D31-00
P6	37	D0	D16#	D31-00

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P7	3	CLK1	IGNNE#	IGNNE#
P7	7	D15	DEP7#	DEP#
P7	9	D14	DEP6#	DEP#
P7	11	D13	DEP5#	DEP#
P7	13	D12	DEP4#	DEP#
P7	15	D11	DEP3#	DEP#
P7	17	D10	DEP2#	DEP#
P7	19	D9	DEP1#	DEP#
P7	21	D8	DEP0#	DEP#
P7	23	D7	RP#	RP#
P7	25	D6	AP1#	AP#
P7	27	D5	AP0#	AP#
P7	29	D4	RSP#	RSP#
P7	31	D3	A35#	A35-32
P7	33	D2	A34#	A35-32
P7	35	D1	A33#	A35-32
P7	37	D0	A32#	A35-32

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P8	3	CLK1	IERR#	IERR#
P8	7	D15	LOCK#	LOCK#
P8	9	D14	BPRI#	BPRI#
P8	11	D13	BR3#	BR#
P8	13	D12	BR2#	BR#
P8	15	D11	BR1#	BR#
P8	17	D10	BR0#	BR#
P8	19	D9	BNR#	BNR#
P8	21	D8	AERR#	AERR#
P8	23	D7	*	
P8	25	D6	*	
P8	27	D5	*	
P8	29	D4	*	
P8	31	D3	*	
P8	33	D2	*	
P8	35	D1	*	
P8	37	D0	*	

* These signals are generated by the preprocessor interface.

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P9	3	CLK1	SMI#	SMI#
P9	7	D15		
P9	9	D14		
P9	11	D13		
P9	13	D12		
P9	15	D11		
P9	17	D10	*	
P9	19	D9	*	
P9	21	D8	*	
P9	23	D7	*	
P9	25	D6	*	
P9	27	D5	PREQ#	PREQ#
P9	29	D4	PRDY#	PRDY#
P9	31	D3	BP3#	BP3#
P9	33	D2	BP2#	BP2#
P9	35	D1	BPM1#	BPM1#
P9	37	D0	BPM0#	BPM0#

* These signals are generated by the preprocessor interface.

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P10	3	CLK1	A20M#	A20M#
The remaining signals on this pod are reserved for future use.				

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P11	3	CLK1	LINT0/INTR	LINT0, INTR
P11	7	D15	D47#	D63-32
P11	9	D14	D46#	D63-32
P11	11	D13	D45#	D63-32
P11	13	D12	D44#	D63-32
P11	15	D11	D43#	D63-32
P11	17	D10	D42#	D63-32
P11	19	D9	D41#	D63-32
P11	21	D8	D40#	D63-32
P11	23	D7	D39#	D63-32
P11	25	D6	D38#	D63-32
P11	27	D5	D37#	D63-32
P11	29	D4	D36#	D63-32
P11	31	D3	D35#	D63-32
P11	33	D2	D34#	D63-32
P11	35	D1	D33#	D63-32
P11	37	D0	D32#	D63-32

IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P12	3	CLK1	LINT1/NMI	LINT1, NMI
P12	7	D15	D63#	D63-32
P12	9	D14	D62#	D63-32
P12	11	D13	D61#	D63-32
P12	13	D12	D60#	D63-32
P12	15	D11	D59#	D63-32
P12	17	D10	D58#	D63-32
P12	19	D9	D57#	D63-32
P12	21	D8	D56#	D63-32
P12	23	D7	D55#	D63-32
P12	25	D6	D54#	D63-32
P12	27	D5	D53#	D63-32
P12	29	D4	D52#	D63-32
P12	31	D3	D51#	D63-32
P12	33	D2	D50#	D63-32
P12	35	D1	D49#	D63-32
P12	37	D0	D48#	D63-32

Repair strategy

The repair strategy for this preprocessor interface is product replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Technologies Sales Office for further information on servicing the board.

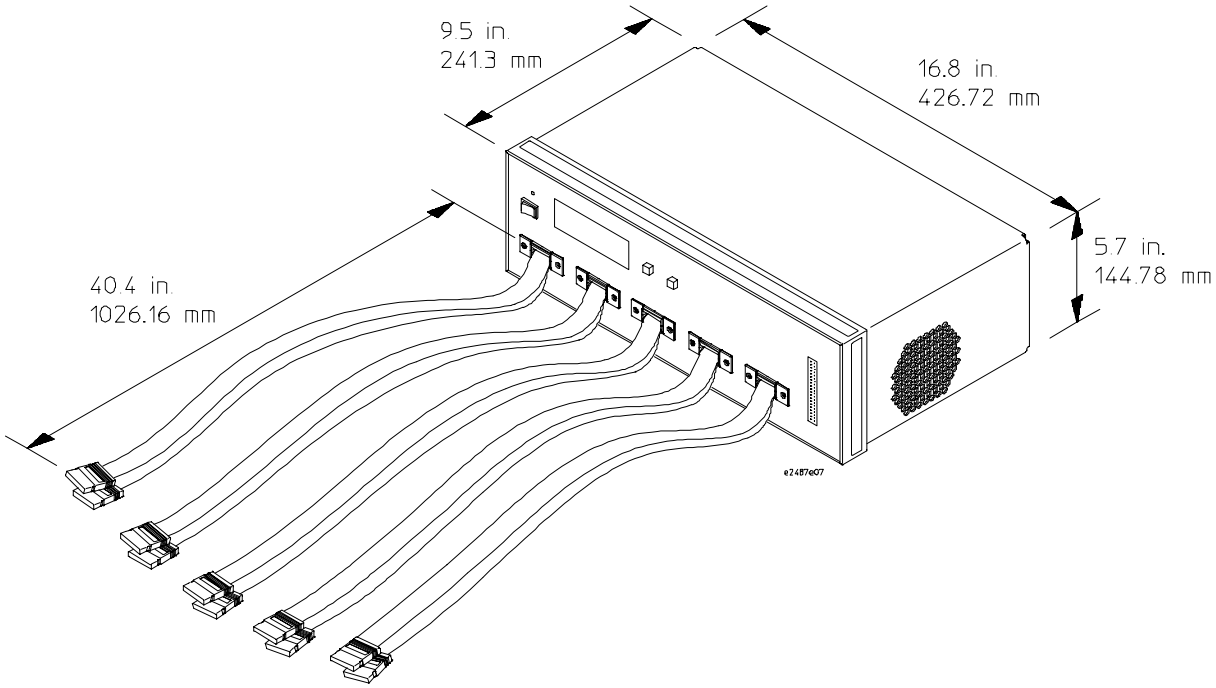
Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

Agilent Part Number	Description
E2487-69002	Rebuilt Preprocessor assembly
E2474-61601	Probe Cable

Physical dimensions

The figure below gives the dimensions for the preprocessor interface. The dimensions are listed in inches and millimeters.



Dimensions

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Agilent Technologies service center.

CAUTION

When you are working with the analyzer, be sure to power down the analyzer, preprocessor interface, and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reconnect all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Check that the logic analyzer threshhold is set for TTL levels.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive Loading" in this chapter for information on other sources of intermittent data errors.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Preprocessor Problems

This section lists problems that you might encounter when using a preprocessor. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Agilent Technologies Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the preprocessor interface, the microprocessor (if socketed) or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the preprocessor and target system.**

  1 Power up the analyzer and preprocessor.

  2 Power up the target system.

  If you power up the target system before you power up the preprocessor, interface circuitry in the preprocessor may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the preprocessor interface are properly rotated and aligned, so that the index pin on the microprocessor (such as pin 1 or A1) matches the index pin on the preprocessor interface.**

- ☐ **Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and are firmly inserted.**

- ☐ **Reduce the number of extender sockets.**

See Also "Capacitive Loading" in this appendix.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and transaction tracker failures.

- ☐ **Ensure that the preprocessor operating mode is correctly set for the measurement you are trying to make.**
- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some preprocessor designs require a full reset to ensure correct configuration.
- ☐ **Ensure that your target system meets the timing requirements of the processor with the preprocessor probe installed.**

  See “Capacitive Loading” in this chapter. While preprocessor loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.
- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the preprocessor interface, or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz, or that have fast edge speeds.

Transaction Tracker/Inverse Assembler Problems

This section lists problems that you might encounter while using the transaction tracker/inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and transaction tracker/inverse assembler correctly, you can proceed with confidence in debugging your target system.

No transaction tracking or incorrect transaction tracking

- ☐ **Ensure that each logic analyzer pod is connected to the correct preprocessor connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and preprocessor cable numbers. Preprocessors must supply address, data, and status information to the analyzer in a predefined order. The cable connections for each preprocessor are often altered to support that need. Thus, one preprocessor might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the A35-32, A31-00, D63-32, D31-00, STAT_1, and STAT_0 format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. See Chapter 2 for more information.

- ☐ **Verify that storage qualification has not excluded storage of all the needed transaction phase information.**

Transaction tracker/inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the transaction tracker/inverse assembler is on the same disk as the configuration files you are loading and is in the same directory on the Agilent Technologies 16500B/C mainframe. For the Agilent Technologies 16505A Prototype Analyzer the transaction tracker must be in the /hp16505/ia directory.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding transaction tracker/inverse assembler for the Pentium II processor. If you delete the transaction tracker/inverse assembler file or rename it, the configuration process will fail to load the transaction tracker/inverse assembler file properly.

  See Chapter 1 for details.

Transaction tracker/inverse assembler errors and warnings

********** ******** (no data displayed in the transaction display)**

It is common for transactions near the end of the acquisition to be clipped such that not all data phases are captured. In this case, any data states which are missing will be indicated by a row of asterisks.

? (appears next to a disassembled instruction)

Branch Trace Messages normally guarantee accurate disassembly. Intel has acknowledged a BTM anomaly in the Pentium II processor where the current BTM target address is okay, but the next BTM causing address is incorrect. The Agilent Technologies 16505A software attempts to work around this problem when performing instruction disassembly, but in some cases may not be able to, in which case it marks the instruction with a question mark. This questionable instruction may have been prefetched but not executed.

<ia notice: long format requires Intel NDA>
<ia notice: non-ReqA info requires Intel NDA>

The features you have tried to access are only available in the restricted version of the Agilent Technologies E2487A. Contact your Agilent Technologies Sales Office for information on obtaining the appropriate Intel non-disclosure forms and software for accessing the restricted features.

<pp error: rcnt invalid -- reset target>
<pp error: scnt invalid -- reset target>

The preprocessor interface hardware tracks the processor bus from reset. If the logic analyzer is turned off while the target is on, or if the preprocessor mode is changed while the target is on, synchronization with the processor bus is lost. To correct this error, reset the target.

<ia error: BTM with target code read missing>

Because disassembly was selected in Preferences dialog, instructions would normally be displayed for the current Branch Trace Message transaction. If the next BTM was found, but the code read at the branch target address for the current BTM is missing, then this error results. To correct this error, disable all processor instruction caches.

<ia warning: next BTM missing -- no disassembly>

Disassembled instructions are displayed as a continuous block for each Branch Trace Message (BTM) transaction. For any given BTM, the software searches for the next BTM to determine which instruction caused a branch to be taken. Near the end of acquisition, the next BTM may be incomplete or missing.

If the number of states to the next BTM exceeds the internal search limit, it will also be treated as missing. The default internal search limit is 8192 states. If you need to change the search limit, contact your Agilent Technologies Sales Office for the procedure.

<ia warning: disassembly requires Branch Trace>

With "Display Disassembly" selected in the Preferences dialog, a code read from the reset vector is treated as a "virtual" Branch Trace Message and normally begins a block of disassembled instructions. This warning indicates that the next "real" BTM is not found. To correct this warning, turn off "Display Disassembly" or enable BTMs on the target system.

<data ECC error: ... >

"Display Read/Write ECC Errors" is selected in the Preferences dialog and an error was detected on D[63:00]# or DEP[7:0]#. This could be a real data integrity problem on the target system, but other more likely reasons are listed below:

-- Probe adapter end not clamped tightly to CPU daughter card.

-- Logic analyzer pods for the D[63:00]# signals are swapped.

-- Data bus ECC checking is not enabled on the target system.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms another measurement module, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Logic Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the Pentium II processor transaction tracker/inverse assembler that is attached to the configuration file. Ensure that the transaction tracker/inverse assembler file is not renamed or deleted.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for the Agilent Technologies 16550B cards. Ensure that your cable connections match the silk screening on the card. Then, repeat the measurement.

See Also The *Agilent Technologies 16550B Logic Analyzer Service Guide*.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ **Verify that the appropriate module has been selected from the Load {module} from File {filename} in the Agilent Technologies 16500B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.**

See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the Agilent Technologies 16500B/C or 16501A frame. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

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This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
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Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

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About this edition

This is the *Agilent Technologies E2487A Preprocessor Interface for Intel IA-32 Processors User's Guide*.

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New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name:	Agilent Technologies
Manufacturer's Address:	1900 Garden of the Gods Road Colorado Springs , CO 80907 U.S.A.

Declares, that the product

Product Name:	IA32 Preprocessor Interface
Model Number(s):	Agilent Technologies E2487A
Product Options:	All

Conforms to the following Product Specifications:

Safety: IEC 1010-1:1990+A1 / EN 61010-1:1993
UL 3111
CSA - C22.2 No. 1010.1:1993

EMC: CISPR 11:1990 /EN 55011 (1991): Group 1, Class A
IEC 555-2:1982 + A1:1985 / EN 60555-2:1987
IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991
IEC 801-2:1991 /EN 50082-1 (1992): 4 kV CD, 8 kV AD
IEC 801-3:1984 /EN 50082-1 (1992): 3 V/m, {1kHz 80% AM, 27-1000 MHz}
IEC 801-4:1988 /EN 50082-1 (1992): 0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC, and carries the CE-marking accordingly.

This product was tested in a typical configuration with Agilent Technologies test systems.

Colorado Springs, June 17, 1997

John Strathman, Quality Manager

European Contact: Your local Agilent Technologies Sales and Service Office or Agilent Technologies GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, 71034 Böblingen Germany (FAX: +49-7031-143143)

Product Regulations

Safety IEC 1010-1: 1990+A1 / EN 61010-1: 1993
UL 3111
CSA-C22.2 No.1010.1:1993

EMC This Product meets the requirements of the European Communities (EC) EMC Directive 89/336/EEC.

Emissions EN55011/CISPR 11 (ISM, Group 1, Class A equipment), IEC 555-3

Immunity

EN50082-1	Performance Code	Notes
IEC 801-2 (ESD) 8kV AD	3	1
IEC 801-3 (Rad.) 3V/m	3	
IEC 801-4 (EFT) 1kV	3	

Performance Codes:
1 Pass - Normal operation, no effect.
2 Pass - Temporary degradation, self recoverable.
3 Pass - Temporary degradation, operator intervention required.
4 Fail - Not recoverable, component damage.

Notes: (none)

Sound Pressure Level Less than 60 dBa